Side-Channel Security

Chapter 3: Trusted Execution Environments and Confidential Computing

Sudheendra Neela

March 13, 2025

Graz University of Technology

Motivation

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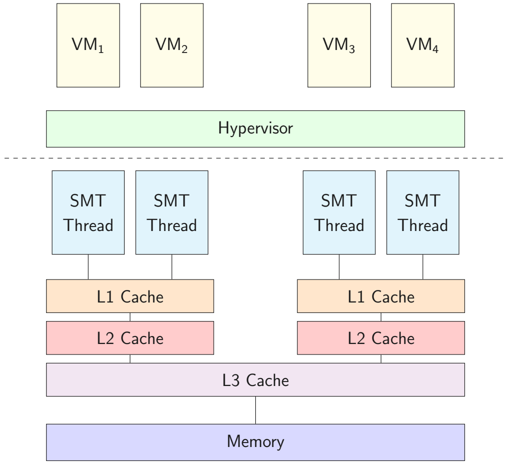
- Key enabler of confidential computing

Virtualization



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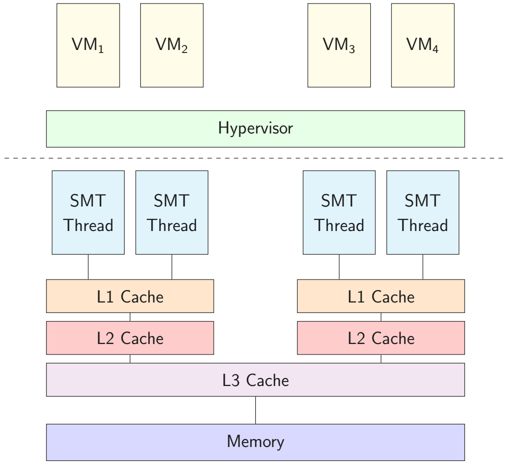

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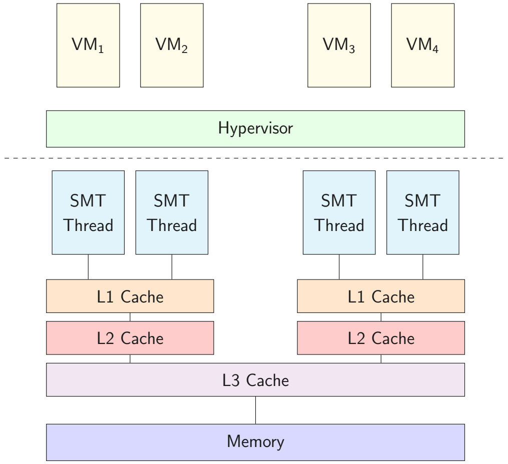

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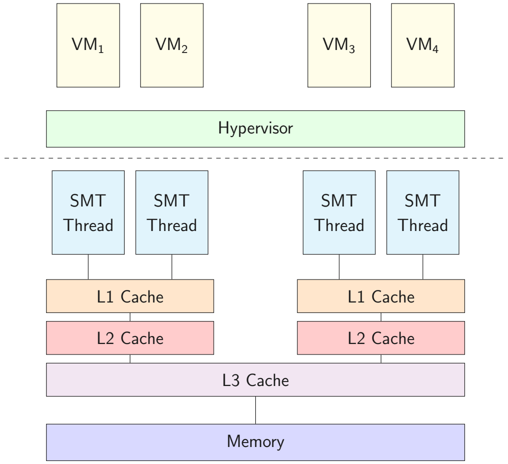

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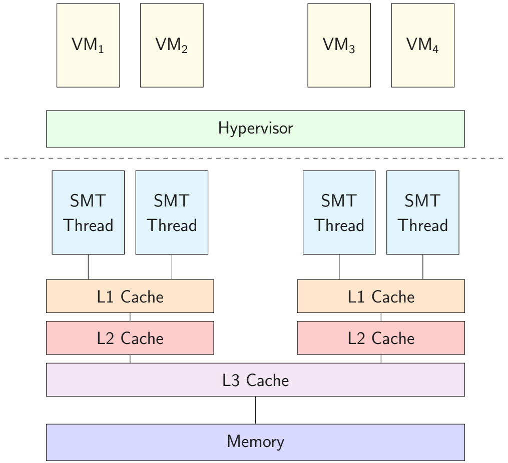

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- Confidential Computing (CoCo): hardware guarantees for secure VM operation

A Simple Correlation Attack [17] (2011)

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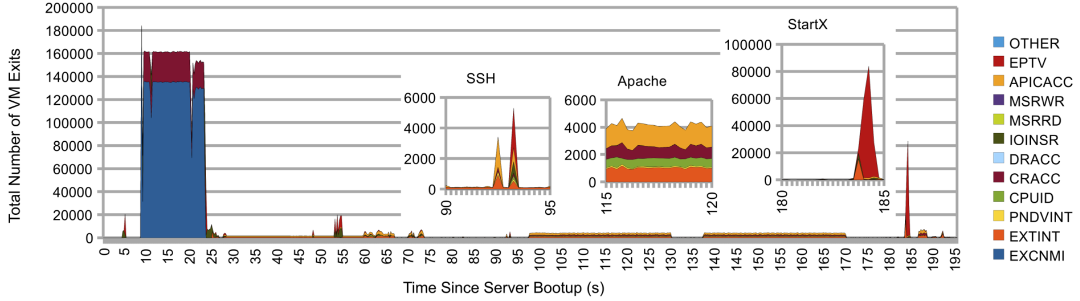

TEE & CoCo Throughout The Years

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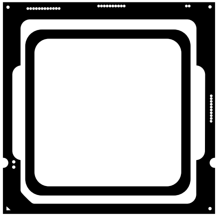
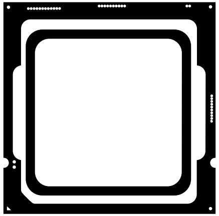
Intel Software Guard Extension (SGX)

Intel SGX Overview



- x86 instruction-set extension

Intel SGX Overview



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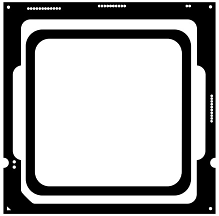

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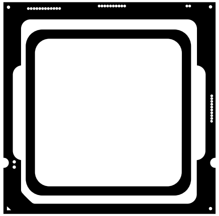

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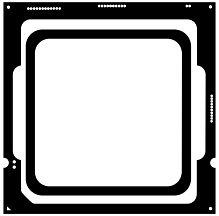

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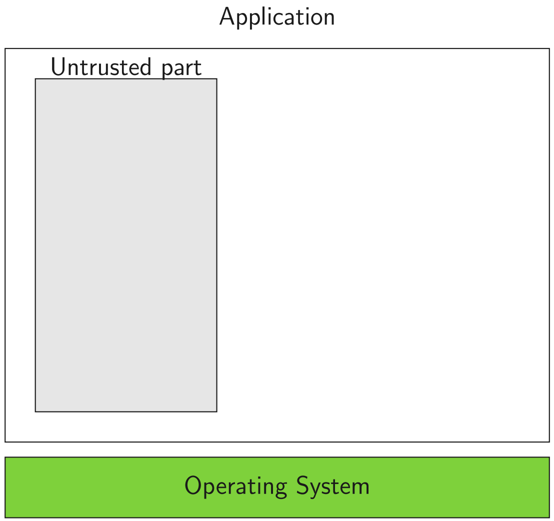
- Enclave has full access to virtual memory of host application

SGX Model



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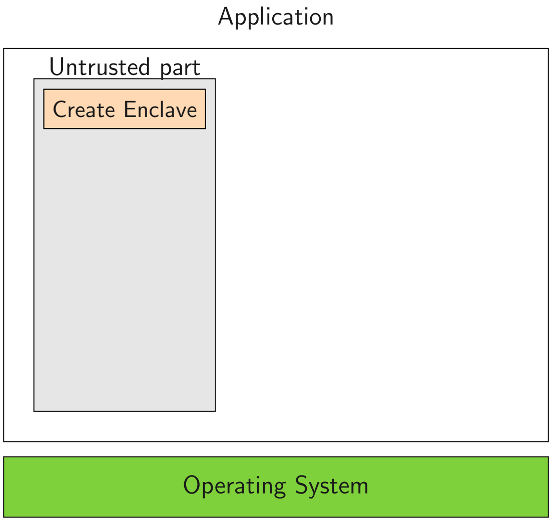
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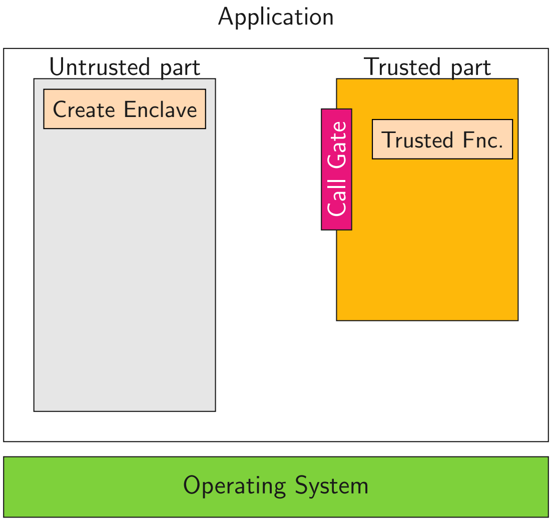
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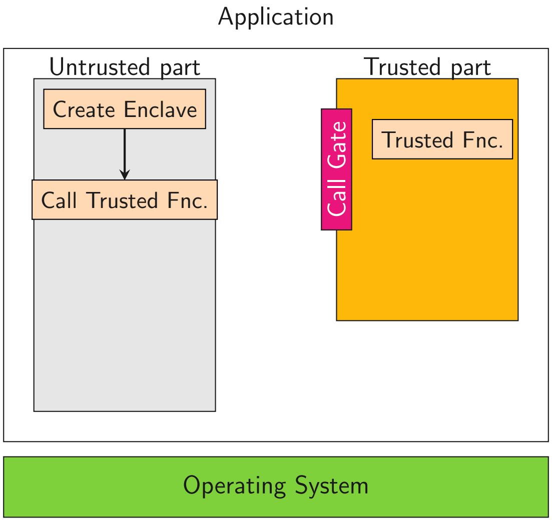
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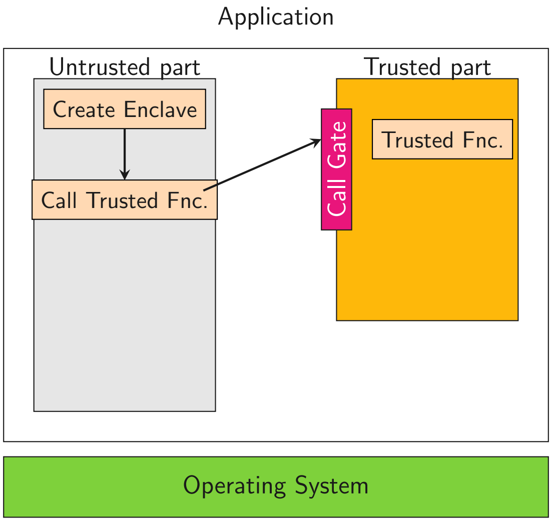
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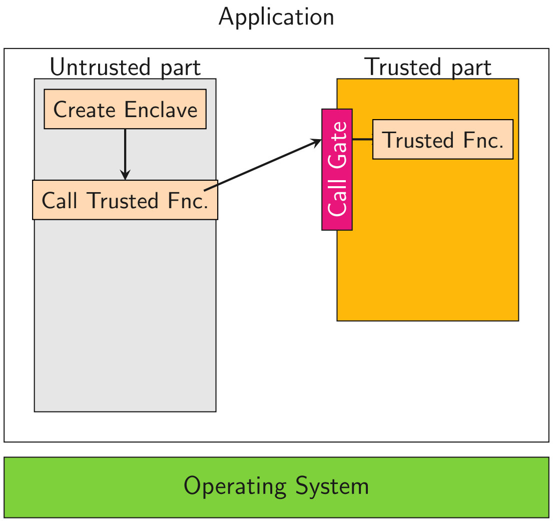
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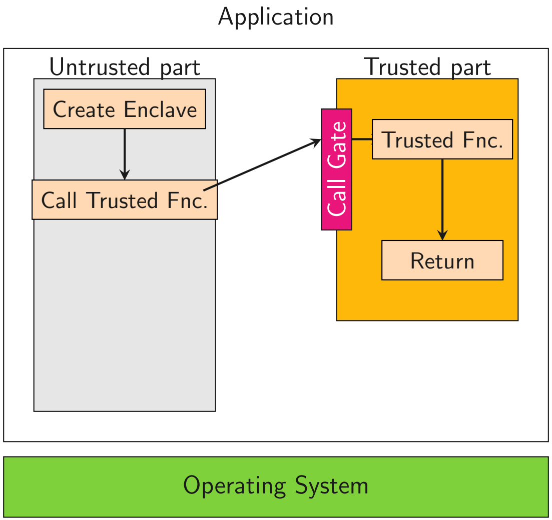
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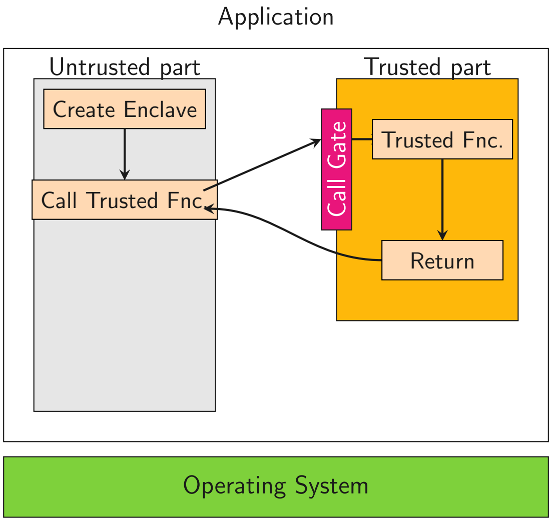
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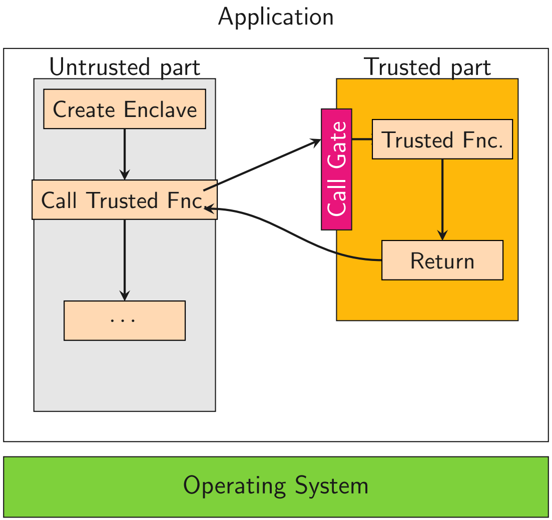
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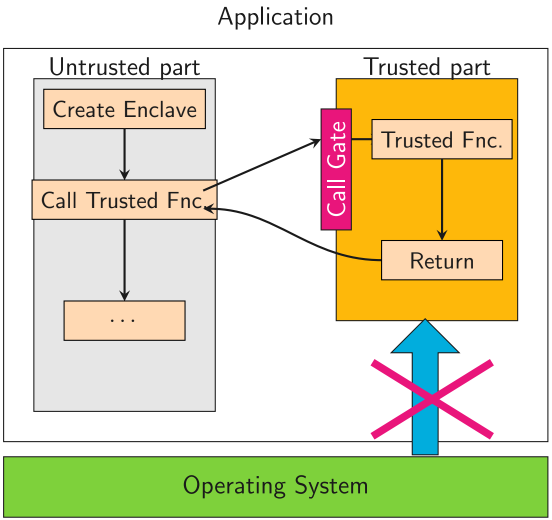
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- Only CPU is trusted

Attack Targets

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Page Table

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Cache Page Table DRAM Network Predictors Interrupt

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Read “SoK: SGX.Fail: How Stuff Gets eXposed” [20]

Side-Channel Attacks on Intel SGX

Controlled-Channel Attacks [24]

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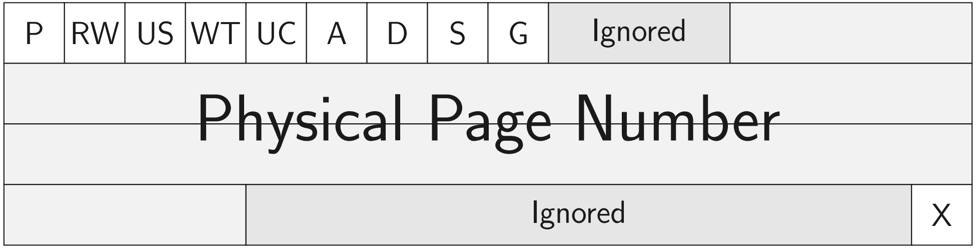
- Granularity: 1 page (4kB)

Stealthier Controlled-Channel Attacks [19, 21]



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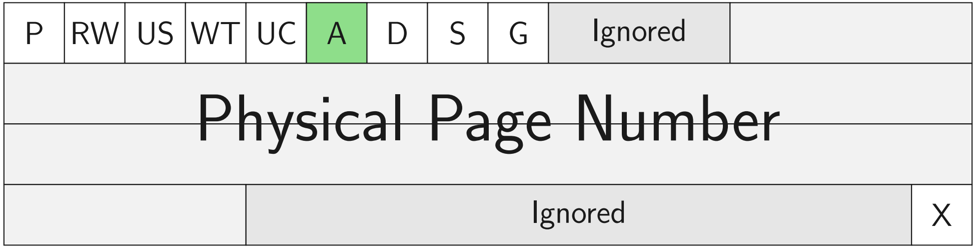

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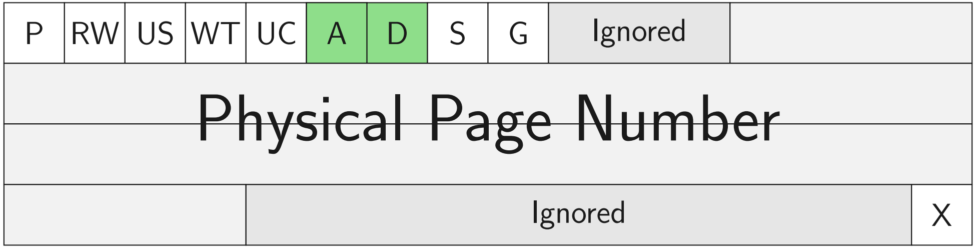

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- Examples: [15], [21], [4], [14]

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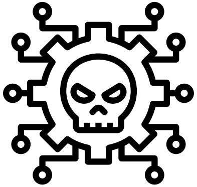

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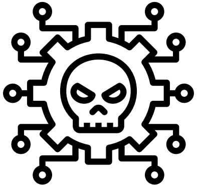

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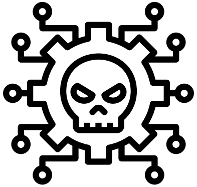

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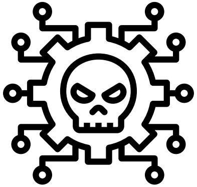

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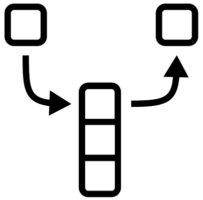
- ...bizarre threat model: Why would an enclave be malicious?

SGX ROP [16]: A Malicious Enclave

- From enclave: host application's memory is accessible, but only if mapped



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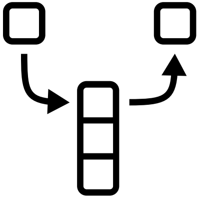

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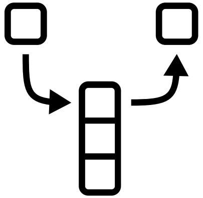

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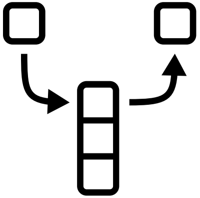

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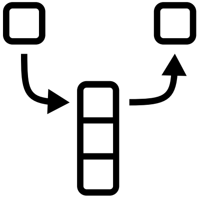

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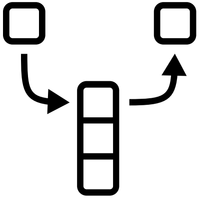

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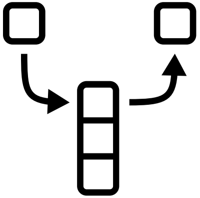
SGX ROP [16]: A Malicious Enclave



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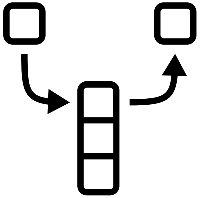

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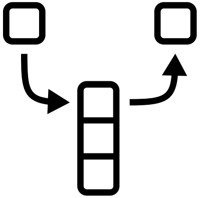

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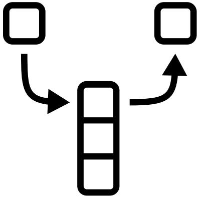

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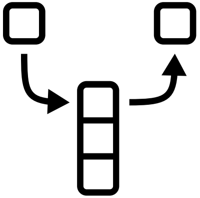

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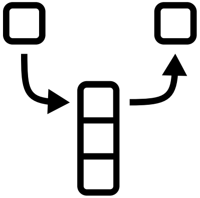

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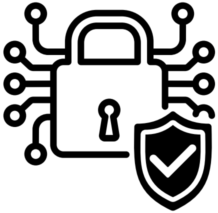
Confidential Computing (CoCo)

Confidential Computing (CoCo) Overview



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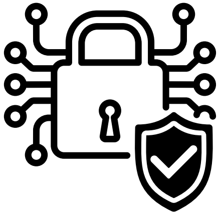

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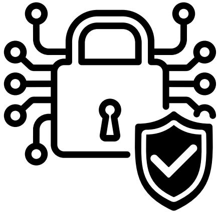

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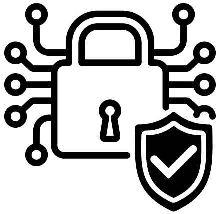

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- Available in server CPUs (Intel Xeon, AMD EPYC)

Attack Targets

Once again, what are some components of a system?

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Cache

Page Table

DRAM

Network

Predictors

Interrupt

CPU Ports

Power

Counters

Fault Attacks (Lecture 4)

Transient Execution (Lecture 3)

Threat Model

- Attacking the CVM: malicious hypervisor

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Side-Channel Attacks on CoCo

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Ciphertext Inference Attacks [12]

VM Save Area

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0x150	16 bytes	CR3 & CR0
0x170	16 bytes	RFLAGS & RIP
0x1D8	8 bytes	RSP
0x1F8	8 bytes	RAX
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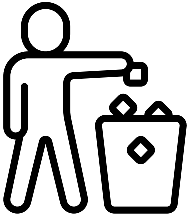
- Change in the CVM's ciphertext: malicious hypervisor can infer the changes of the corresponding plaintext
- Build a dictionary of plaintext-ciphertext pairs for targeted registers

CacheWarp [25]



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CacheWarp [25]

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- How can a malicious hypervisor exploit this?

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11   mov $0x0,%eax
12   call 1158 <ret0>
13   jmp 116f <main+0x8>
```

Cache:

main:6

Memory:

main:6

Registers:

EAX: 0

CacheWarp [25]

```c
int ret1() {
  return 1;
}
int ret0() {
  return 0;
}
int main() {
  while(1){
    if (ret1() == 0){
      printf("Win!");
    }
    ret0();
  }
}
```

```
main:
  push %rbp
  mov %rsp,%rbp
  mov $0x0,%eax
  call <ret1>
  test %eax,%eax
  jne 118c <main+0x25>
  lea 0xe80(%rip),%rax
  mov %rax,%rdi
  call <printf@plt>
  mov $0x0,%eax
  call 1158 <ret0>
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```

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Memory:

$\boxed{\text{main:6}}$

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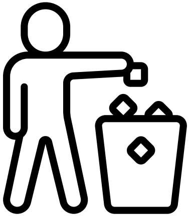

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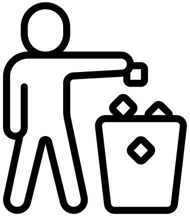

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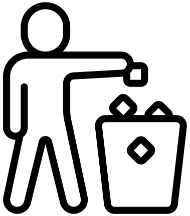

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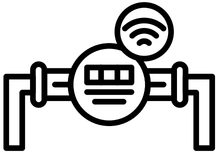
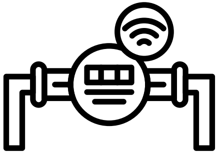
  - UID 0: root

CounterSEVeillance [6]



- CPU provides hardware performance counters:

CounterSEVeillance [6]



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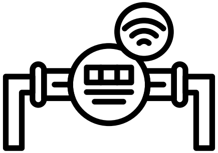

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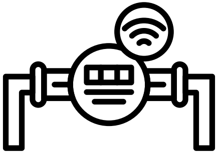

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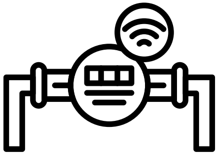

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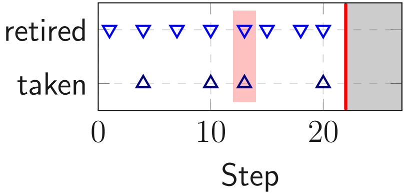
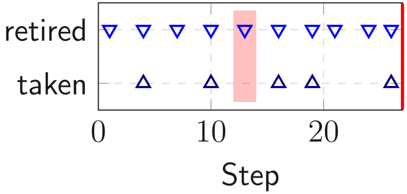
CounterSEVeillance [6]

```
char time_str[data->digits+1];
memset(time_str, 0, data->digits+1);
for (size_t i=0; i<data->digits; i++) {
  if (key[i] != time_str[i])
    return OTP_ERROR;
}
return OTP_OK;
```





Limitations & Solutions

Some limitations

- No shared memory

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Some limitations

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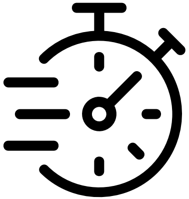
- No syscalls (SGX)

[a] AMD SEV-SNP and Intel TDX now have secure timers

Timer



- We can build our own timer [13, 15]

Timer

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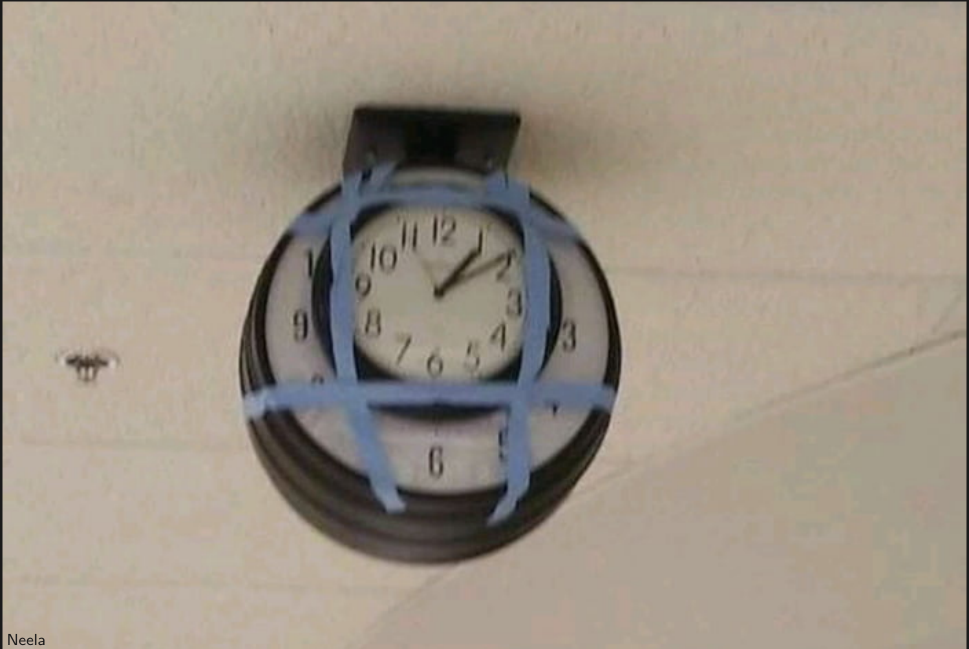
- Start a thread that continuously increments a global variable

Timer

- We can build our own timer [13, 15]
- Start a thread that continuously increments a global variable
- The global variable is our timestamp


Neela

ARE YOU REALLY EXPECTING TO
OUTPERFORM THE HARDWARE COUNTER?
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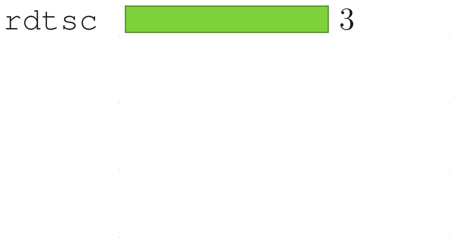
Self-built Timer

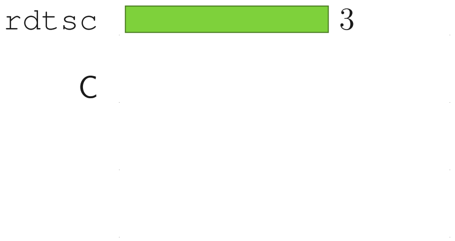
CPU cycles one increment takes



```
timestamp = rdtsc();
```

Self-built Timer

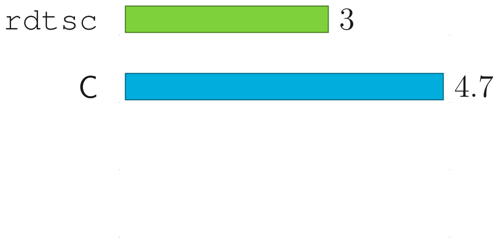
CPU cycles one increment takes



```
while(1) {
  timestamp++;
}
```

Self-built Timer

CPU cycles one increment takes



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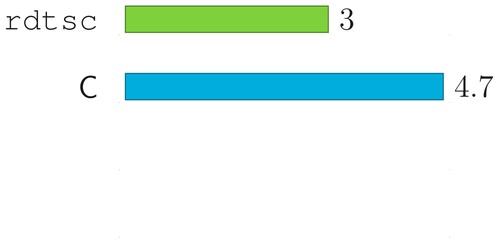

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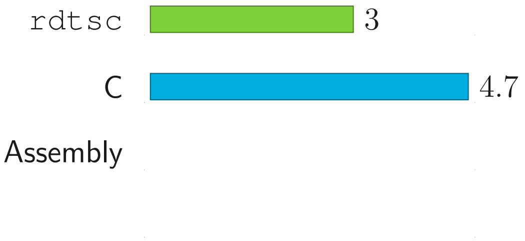

```
mov &timestamp, %rcx
  1: incl (%rcx)
  jmp 1b
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Self-built Timer

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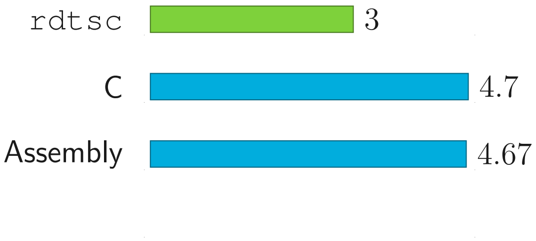

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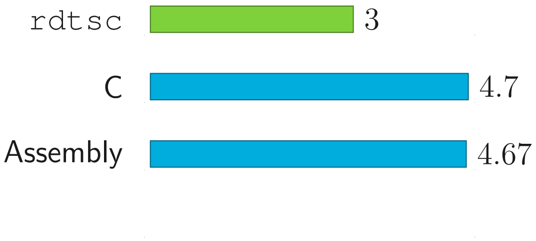

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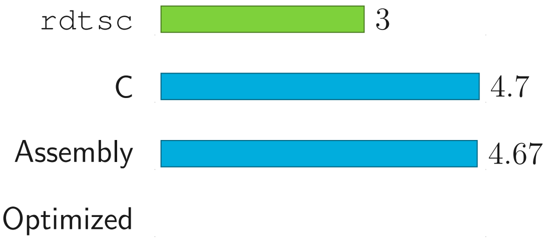

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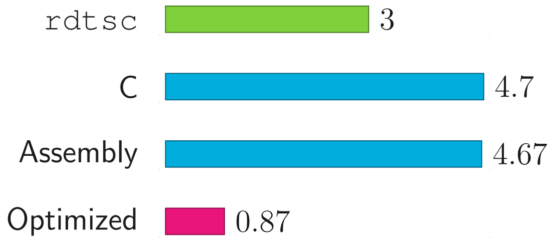

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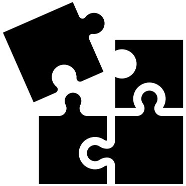
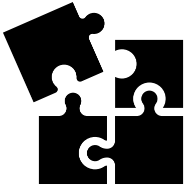
Combining Everything: Malware Guard Extensions (on SGX) [15]



1. Use the counting primitive to measure DRAM accesses

Combining Everything: Malware Guard Extensions (on SGX) [15]



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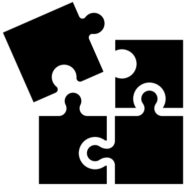
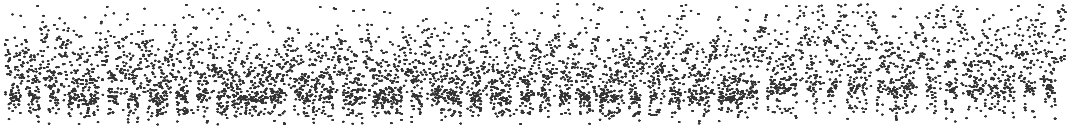


1. Use the counting primitive to measure DRAM accesses
2. Use DRAM side-channel to build eviction set
3. Mount Prime+Probe on the buffer containing the multiplier

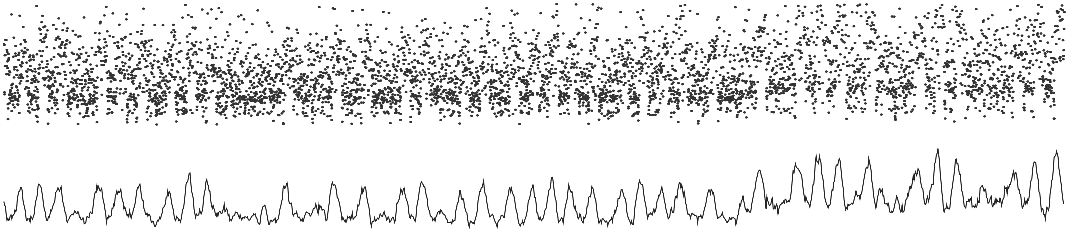
Measured Trace

Raw Prime+Probe trace...



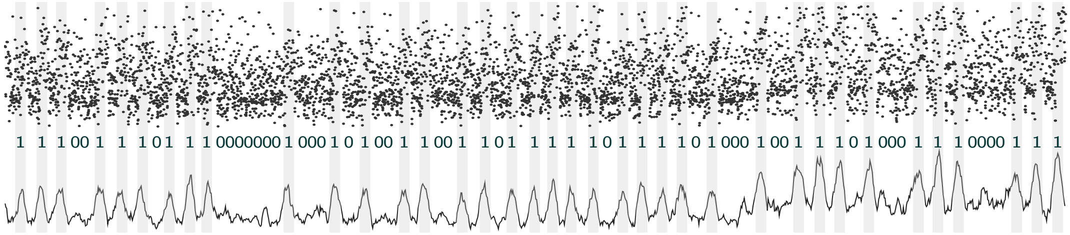
Measured Trace

...processed with a simple moving average...

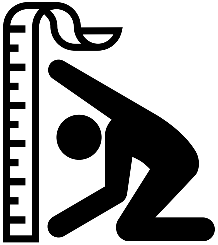


Measured Trace

...allows to clearly see the bits of the exponent



Single-Stepping [18, 23]



- CVM / Enclave: executes many instructions until support from the hypervisor / host is required

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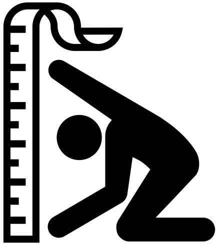

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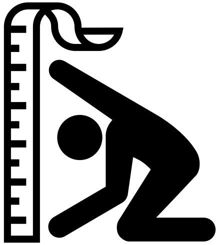

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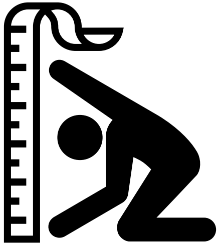

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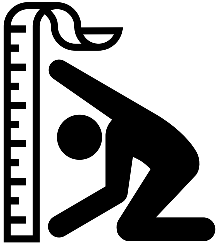

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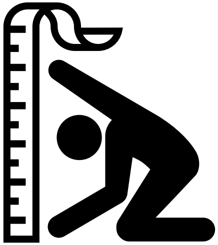

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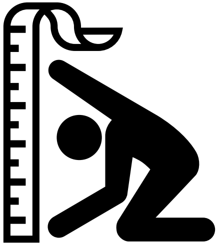

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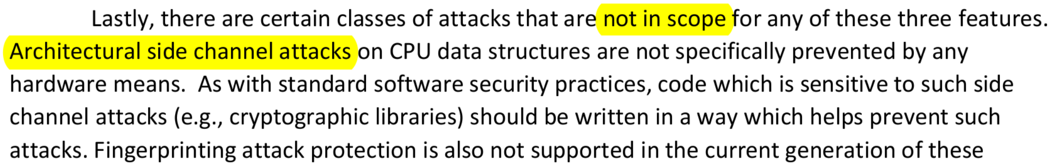
  - TSC-deadline

Conclusion


Lastly, there are certain classes of attacks that are not in scope for any of these three features. Architectural side channel attacks on CPU data structures are not specifically prevented by any hardware means. As with standard software security practices, code which is sensitive to such side channel attacks (e.g., cryptographic libraries) should be written in a way which helps prevent such attacks. Fingerprinting attack protection is also not supported in the current generation of these

- TEEs / CVMs developed to protect sensitive information/critical code execution

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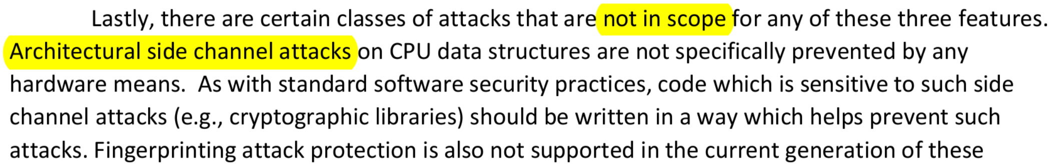
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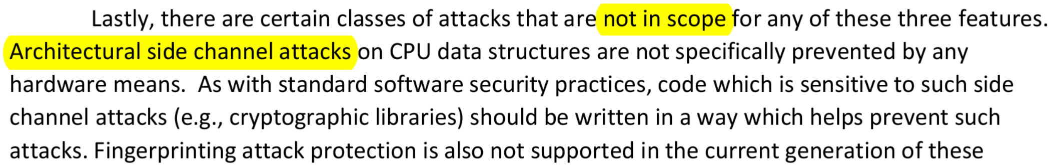
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- TEEs / CVMs developed to protect sensitive information/critical code execution
- Allow for a very powerful threat model: Malicious hypervisor
- SCAs often not "out of scope"

Side-Channel Security

Chapter 3: Trusted Execution Environments and Confidential Computing

Sudheendra Neela

March 13, 2025

Graz University of Technology

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