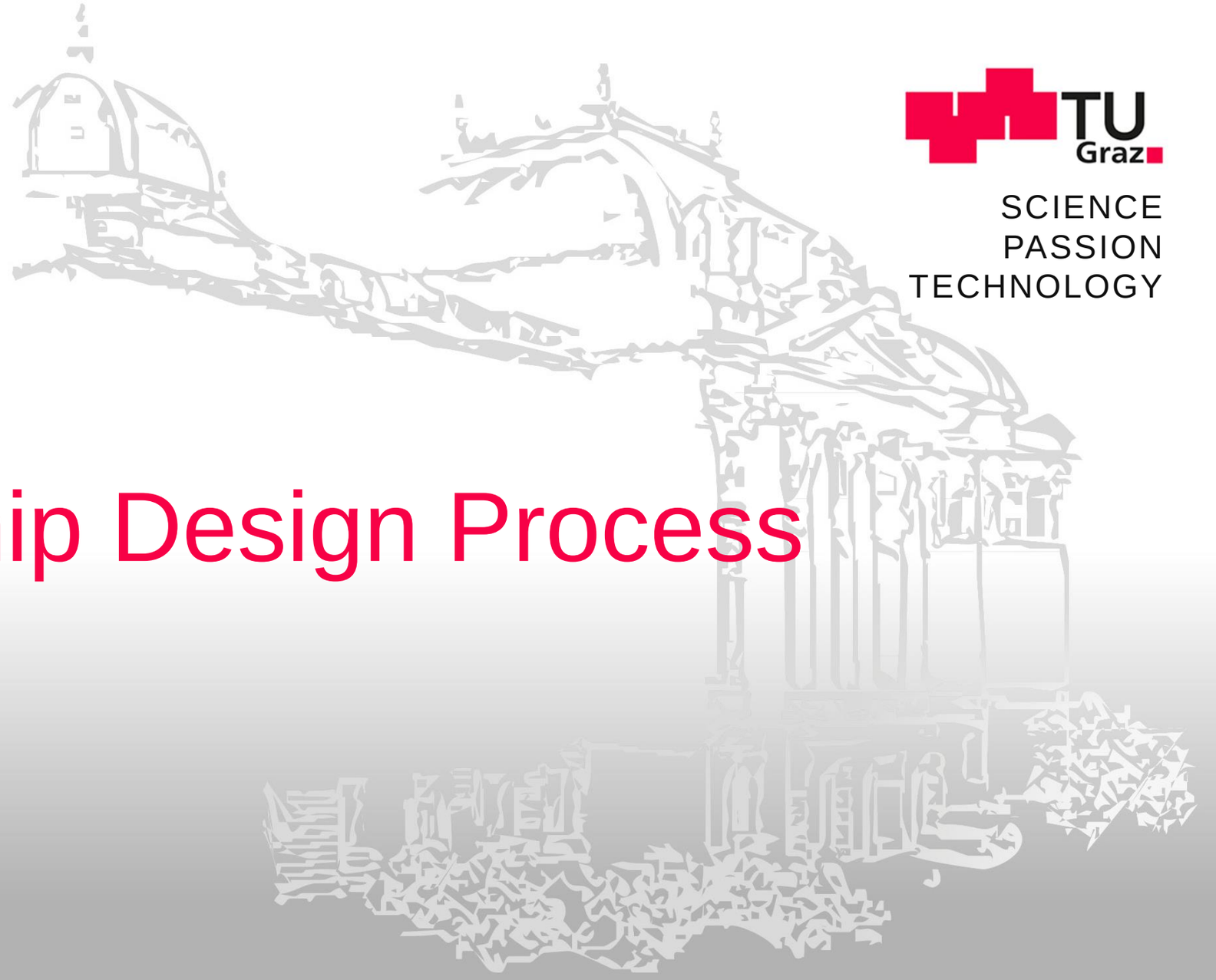


TU Graz

SCIENCE
PASSION
TECHNOLOGY

System-on-Chip Design Process

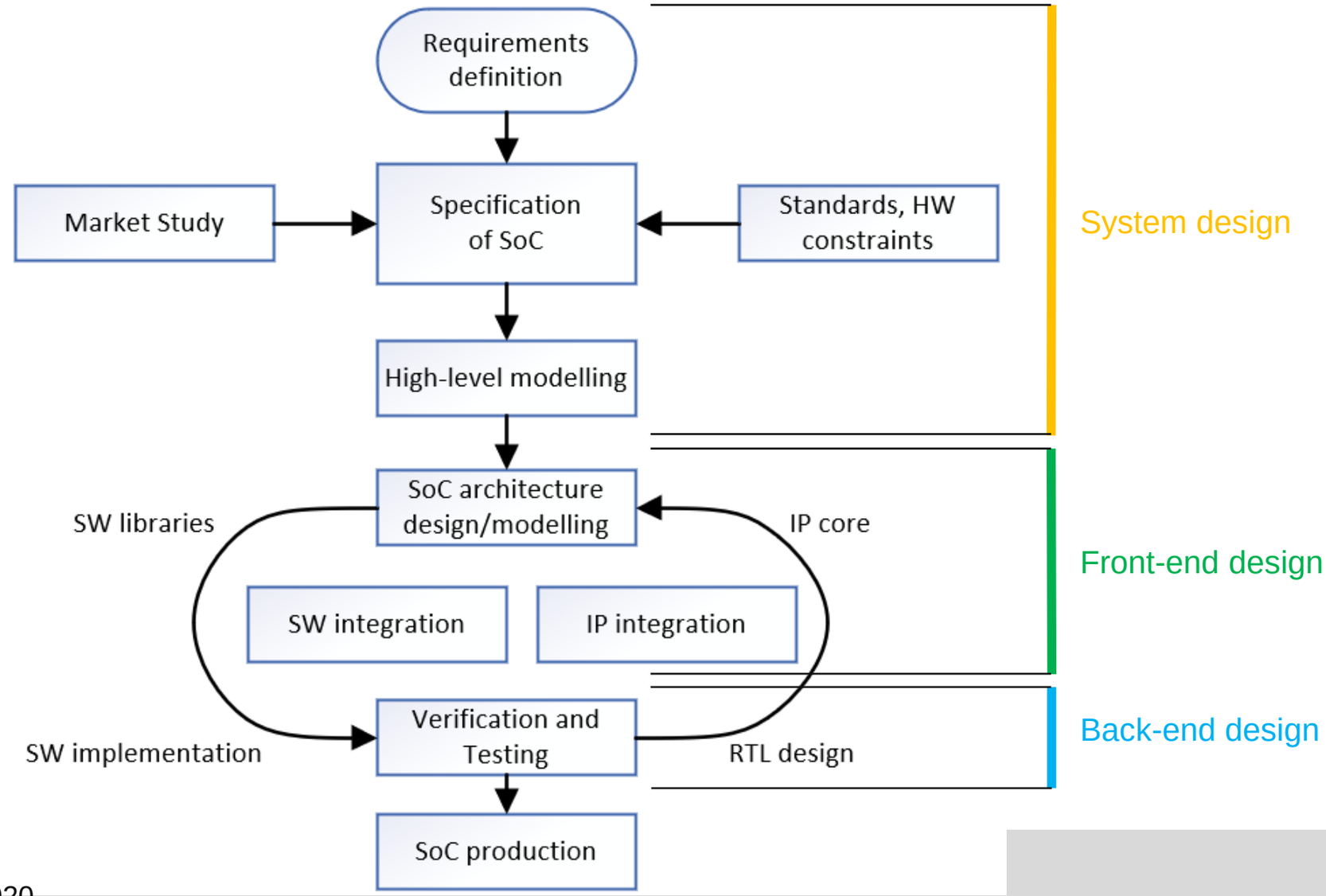
Dominik G.

Wednesday, October 28, 2020

Content

- SoC Design Process
- Involved parties in SoC development

System-on-Chip (SoC) Design Process



IP core – Intellectual property core

- Predefined, designed/verified, reusable building block
  - For ASIC or FPGA designs
- Soft IP
  - Verilog/VHDL or netlist
- Hard IP
  - GDSII
- Examples
  - UART, CPUs, CAN IP-core

Requirements definition

- Explicit requirements
  - Functional specifications: complying to standards (IEEE, …)
- Implicit requirements
  - Examples: very low power consumption, occupy less area, fast response

Specification

- Again: functional and implicit
  - Functional: must be met
  - Implicit: become USP (unique selling proposition)
- Required for hardware and software
  - Functionality, timing, performance
  - Hardware:
    - Interfaces, area, power dissipation
  - Software:
    - Interfaces, SW structure, kernel

Specification

- Executable specification
  - Abstract model for HW and/or SW
  - High-level: SystemC, C, C++
  - Low-level: Verilog or VHDL

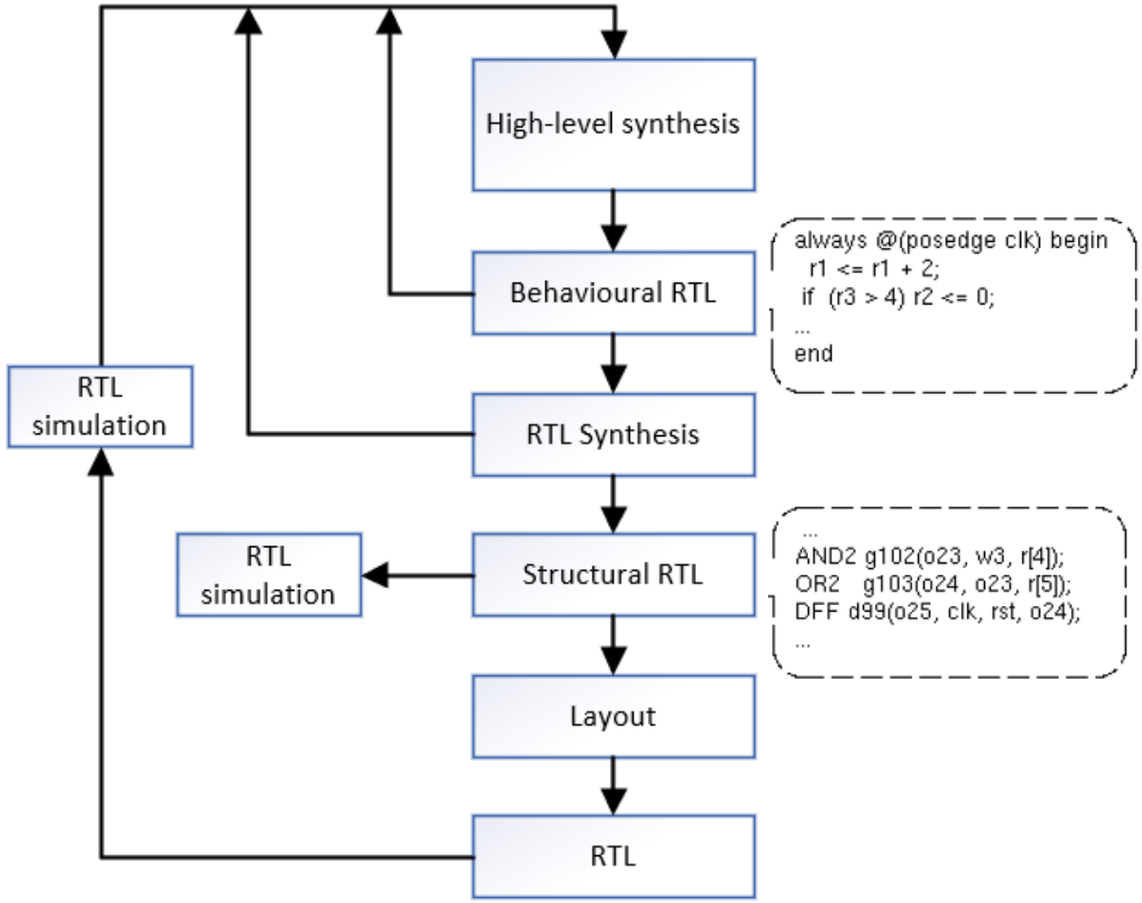
High-level modelling

- Architecture modelling
  - HW/SW partitioning
- Software modelling
  - Algorithmic model
- Hardware modelling

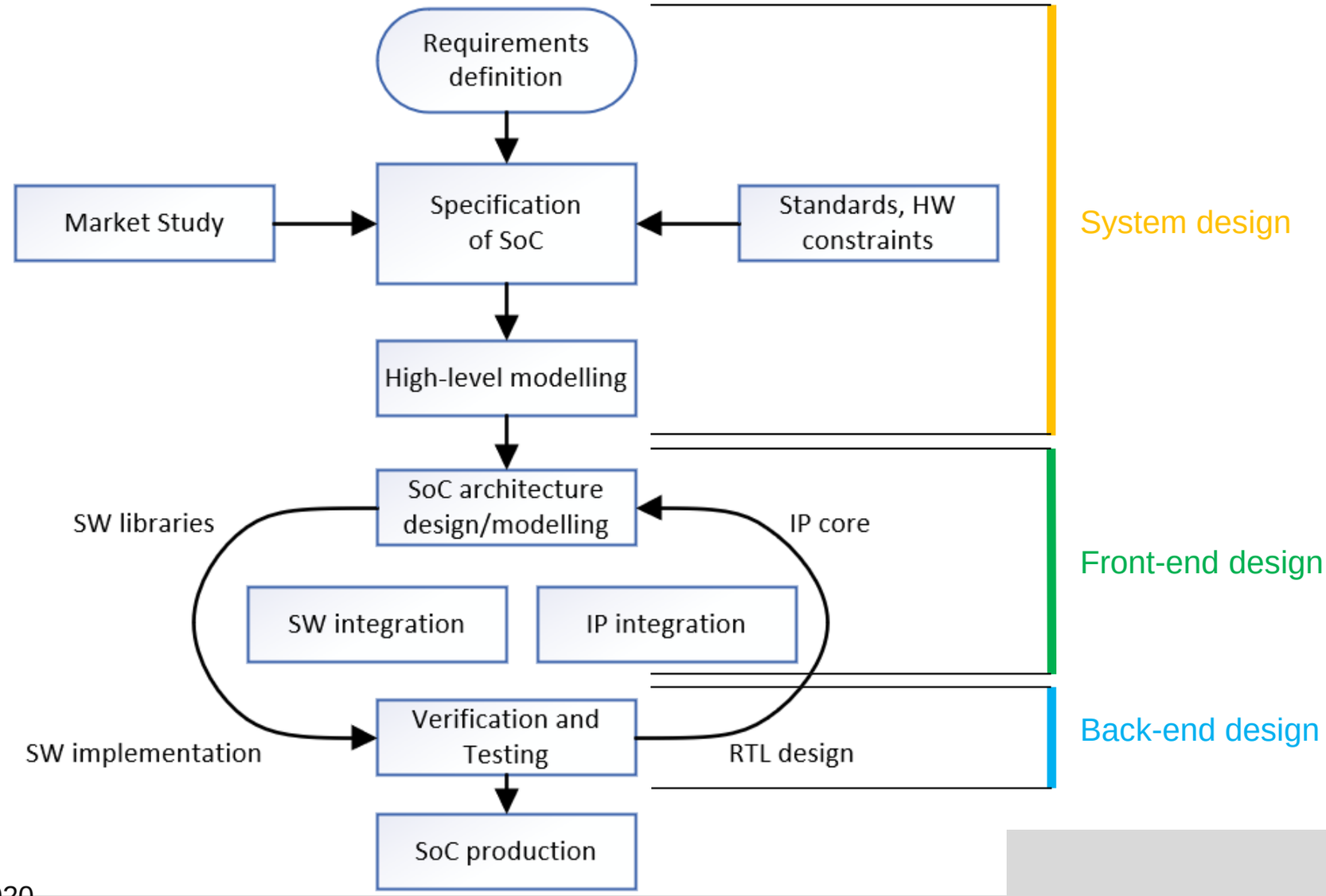
SoC architecture design

- Including design-for-test (DFT)
- Integrating IP cores and SW
- HW:
  - RTL design
  - Simulation
  - Synthesis
  - Power optimization

[5]

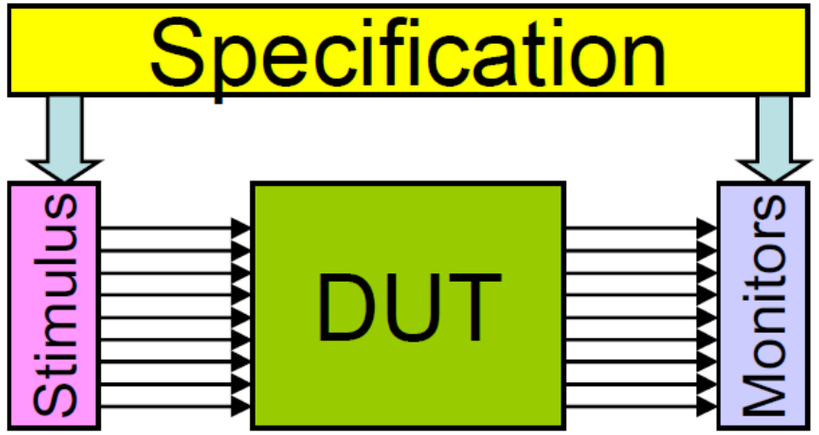


System-on-Chip (SoC) Design Process



Back-end design – Verification and Testing

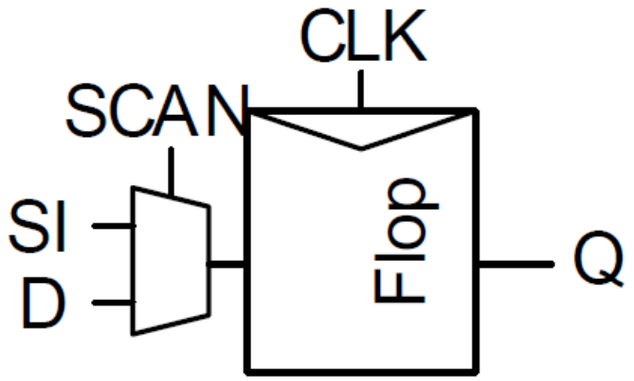
- Requirements fulfilled?
- Various checks
  - Design-rule, electrical, timing-analysis, etc.
- Simulation
  - Test vectors
- HW/SW Co-simulation

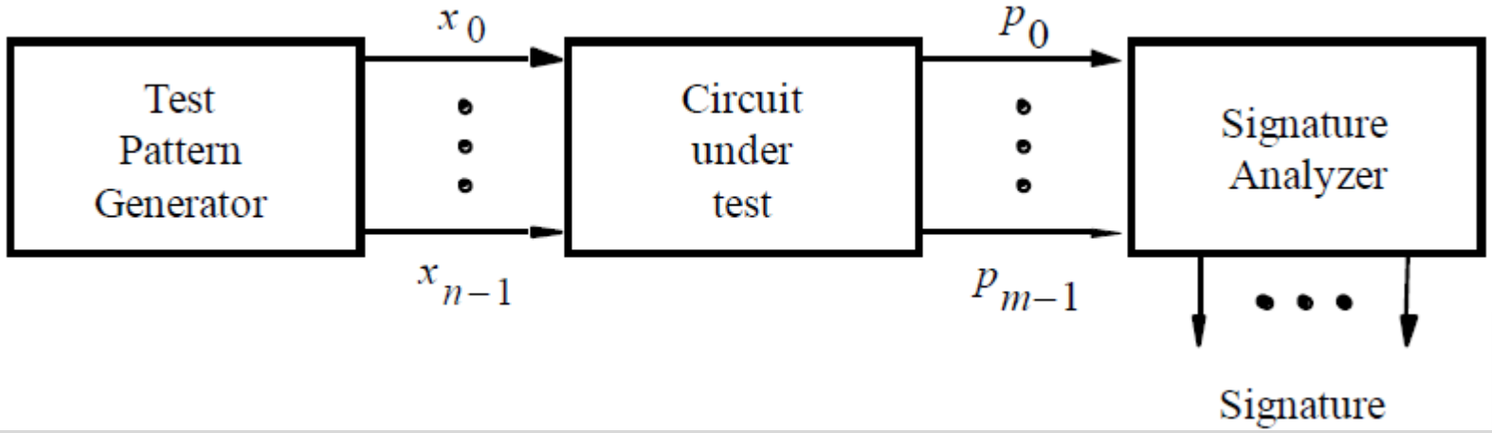


[1]

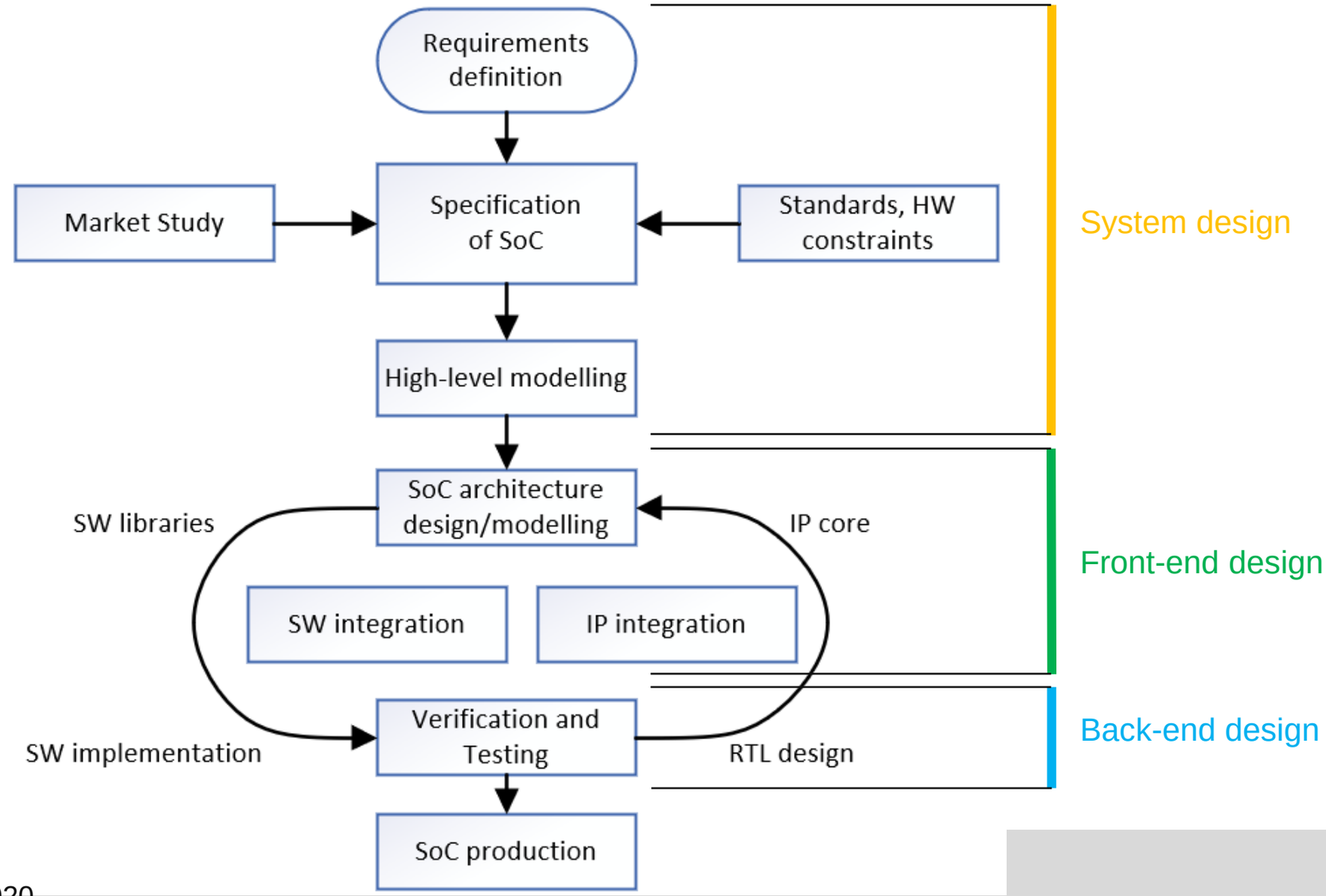
Back-end design – Verification and Testing

- Design-for-testability
  - Add internal test points
  - Scan design
    - Transforming Flipflops into shift register
    - Good CAD tool support
    - ATPG – Automatic test pattern generation
  - **B**uilt **I**n **S**elf **T**est

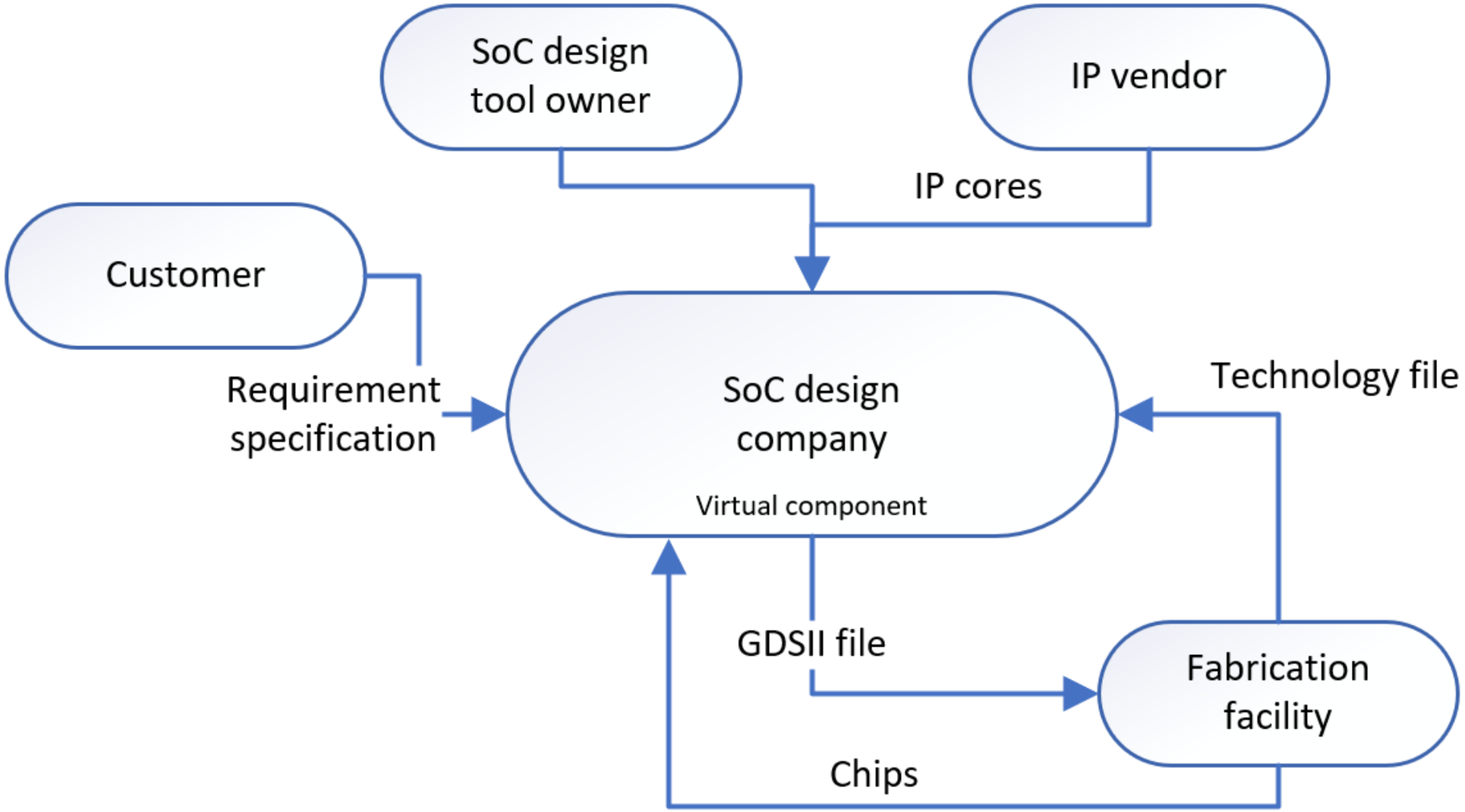




System-on-Chip (SoC) Design Process



Involved parties in System-on-Chip

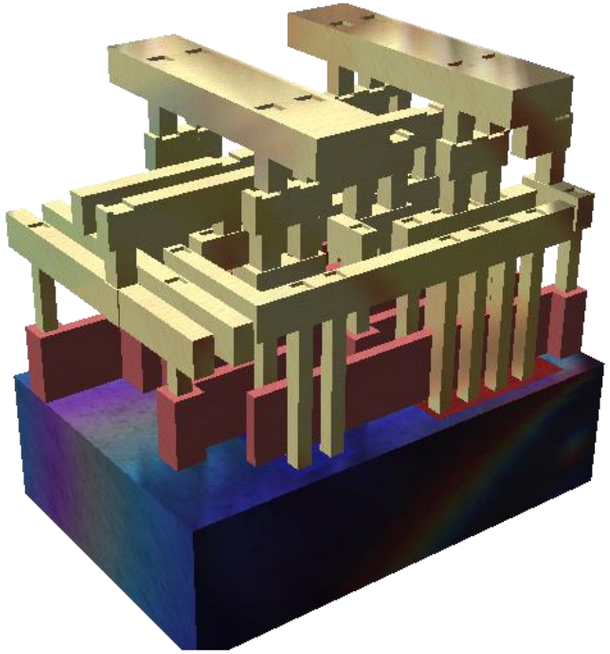


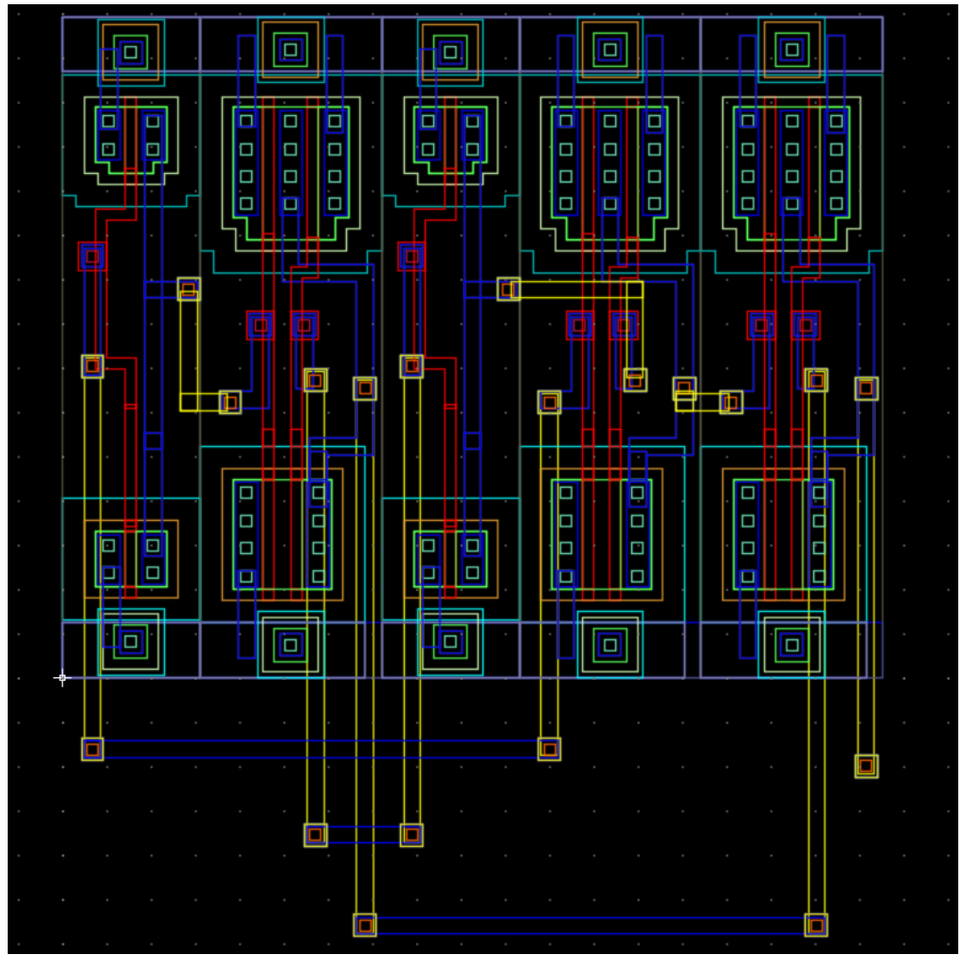
Technology File

- Contains process specific properties
- Available metals
- Thickness, width, design rules, etc.

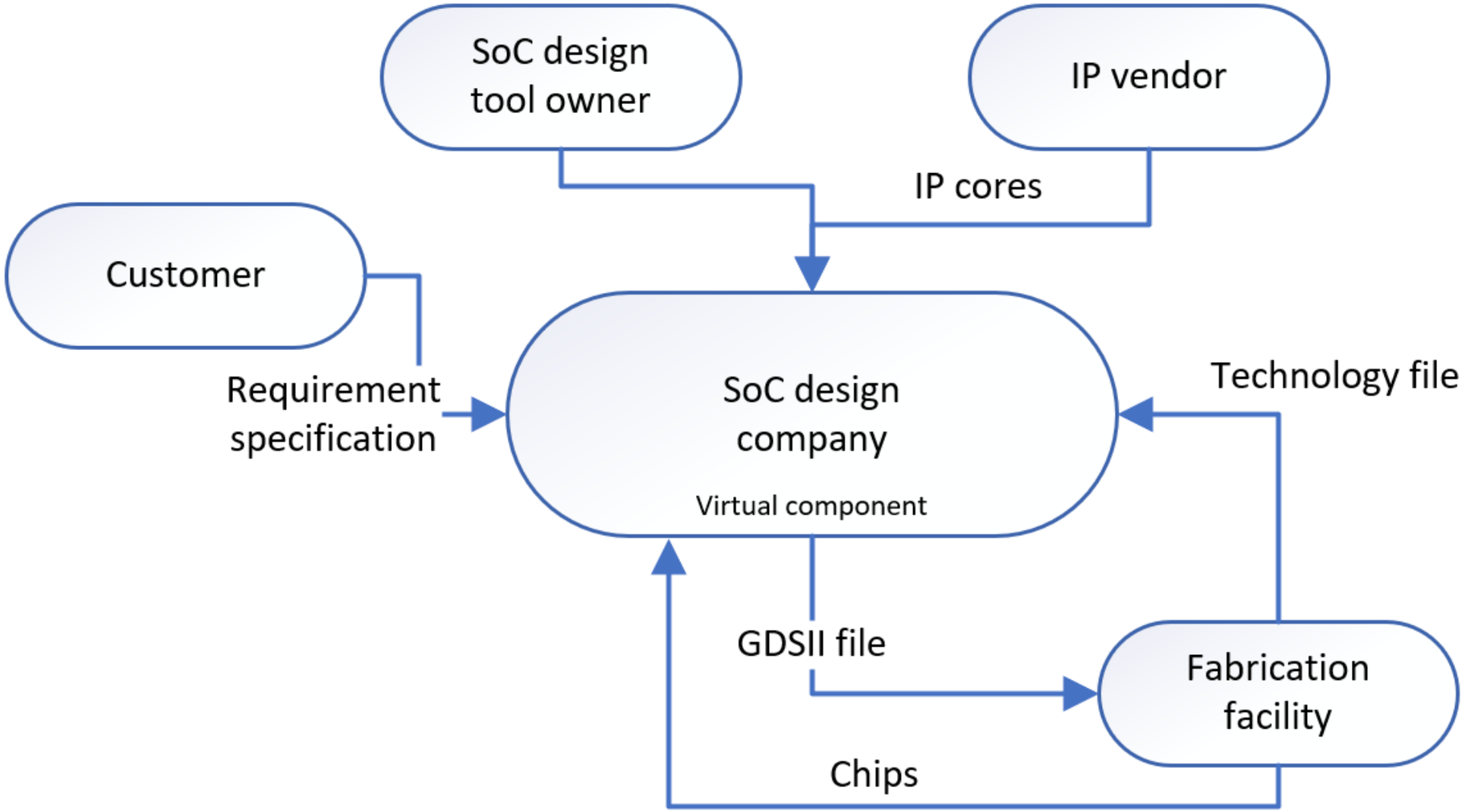
GDSII (GDS2) Files

- **G**raphic **D**esign **S**ystem (1970s)
- Binary files





Involved parties in System-on-Chip



Literature

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- [3] Wayne Wolf, 2009, Modern VLSI Design – IP-Based Design, Fourth Edition. https://docs.google.com/viewer?a=v&pid=sites&srcid=dmVudXNpY3Qub3JnfGVjLWJtLXZsc2ktMTYxMDA0fGd4OjQ5MDNkN2RhOTNlYWYzZTg
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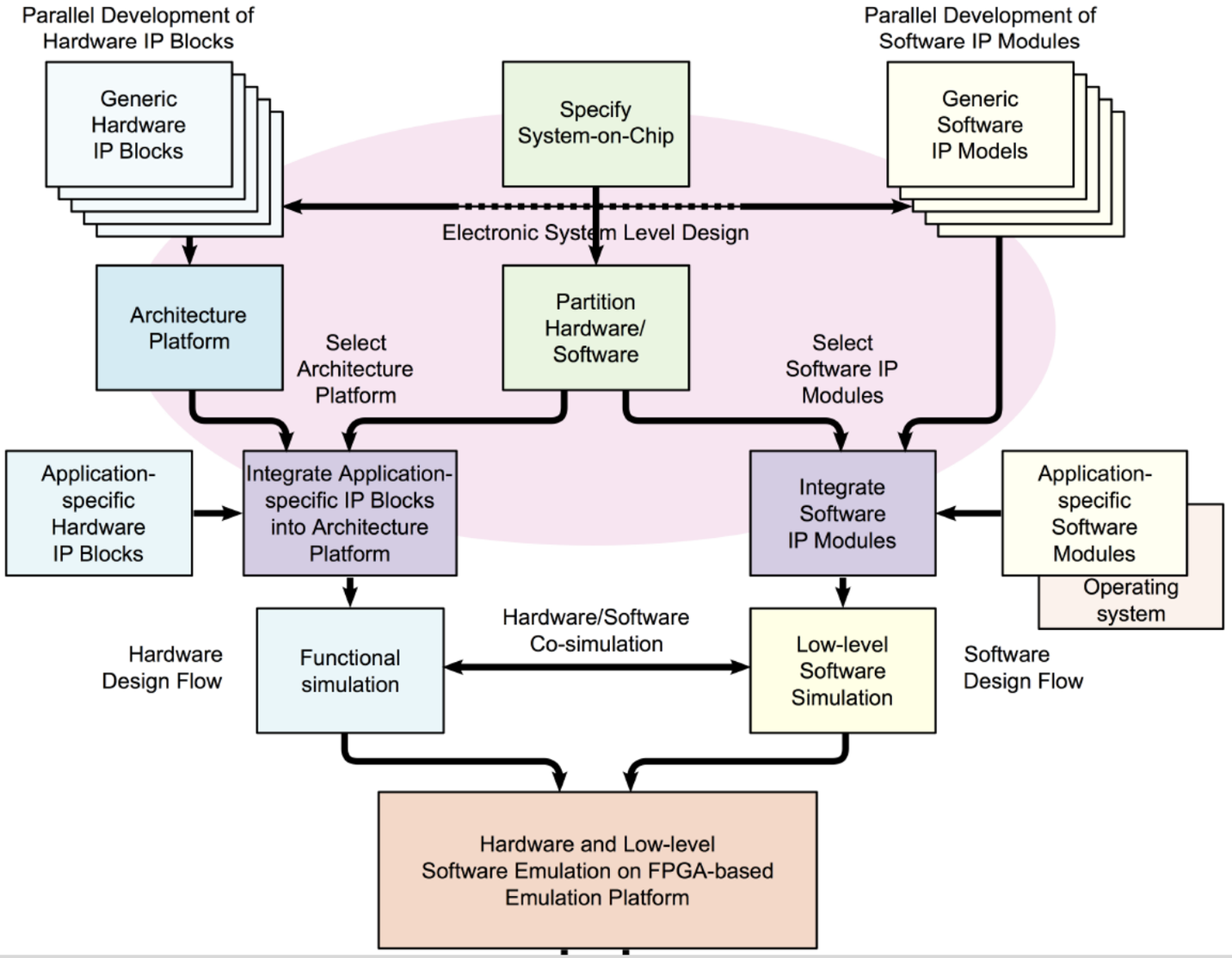
- [5] Dr. David J. Greaves, System on Chip Design and Modelling, University of Cambridge Computer Laboratory Lecture Notes, Part 2, 2015/2016
- [6[Guillaume Delbergue, Advances in SystemC/TLM Virtual Platforms : Configuration, Communication and Parallelism, 2017. https://www.researchgate.net/publication/324792444_Advances_in_SystemCTLM_Virtual_Platforms_Configuration_Communication_and_Parallelism

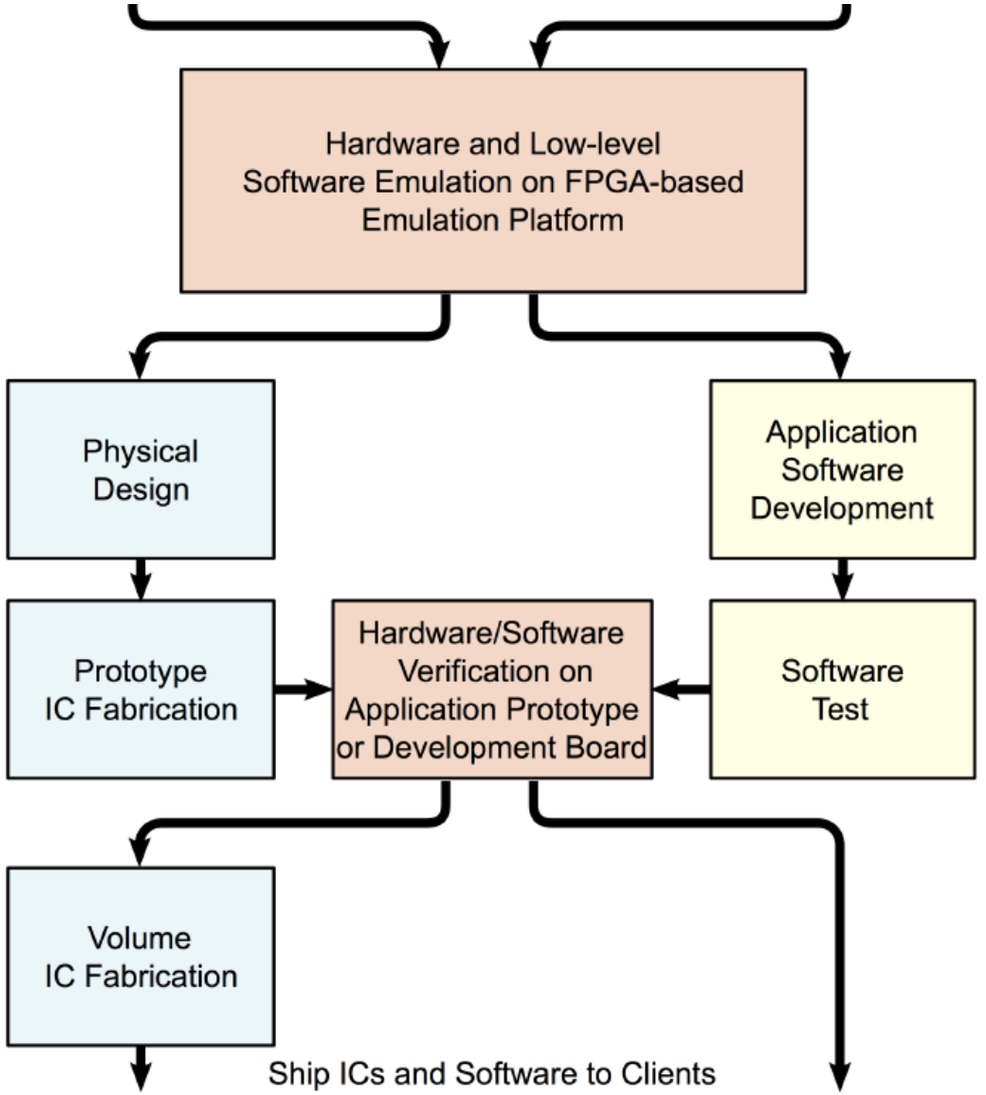
Questions?

- Another view on the design process



[6]

- Another design process (2)



[6]

• Real world example – Philips Viper digital video chip

- Used for digital television
- 2 CPUs (TriMedia & MIPS), IO-devices, DRAM memory controller
- Design
  1) Specification: Design should meet Philips DVP standard
  2) IPs used: TriMedia CPU, MIPS CPU, and one analog block
  3) Register-transfer design
     - High-bandwith peripherals → Philips DVP standard for DMA
     - Low-bandwith peripherals → Philips PI bus standard
     - Fully scan-testable [4]

- Real world example – Philips Viper digital video chip

4) Verification of the design at RTL and gate-level
5) Timing checks
6) Other checks
    - Design rule checks, removing antennas, etc.