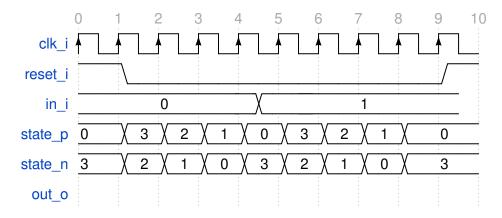
The use of examination aids (e.g., calculators) is prohibited. Answers can be given in German or English. Please refrain from using lead pencils and red ink pens.

Grading scale: 00–25: insufficient 26–31: sufficient 32–38: satisfactory

39–44: good 45–50: very good

Q1. (10 points) **Finite State Machine:** Consider the FSM provided in the timing diagram below. The three top-most signals are 1-bit signals. The three signals at the bottom are 2-bit signals. in\_i is an input signal for this FSM and state\_p is the current state. state\_n and out\_o are outputs of the next state logic and output logic respectively.



- (a) Give the two logical formulas of the next state logic.
- (b) The output logic is defined in Verilog as below. Add the missing out\_o line in the timing diagram (reminder: LSB is at index 0).

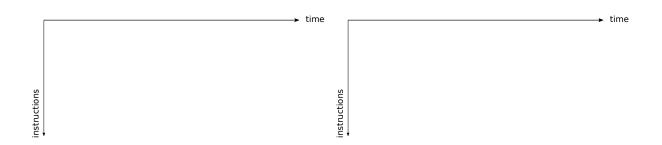
$$\begin{aligned} \mathsf{out\_o}[0] &= (\mathsf{state\_p}[0] \lor \mathsf{state\_p}[1]) \lor \neg \mathsf{in\_i} \\ \mathsf{out\_o}[1] &= \mathsf{state\_p}[0] \land \neg \mathsf{state\_p}[1] \end{aligned}$$

- (c) Draw the ASM diagram of this machine.
- (d) Which type of Finite State Machine is this FSM? What is the name of the other type? What is their difference?

## Q2. (10 points) **Pipelining:**

- (a) Explain the motivation and concept of pipelining based on the following example. You have a single cycle machine with a critical path of 600ps. You are able split the path into three pipeline stages of 200ps each. What does it mean to insert a pipeline stage? Explain how this leads to a speedup. How much is the speedup (assuming a full and ideal pipeline)?
- (b) Assume the three pipeline stages IF, ID (includes reading the operands from the register file), and EX. This pipeline executes the four instructions below. Explain the problem arising in the pipeline with this code snippet. Explain two approaches to resolve this problem.
- (c) Complete the diagrams below for both approaches and show which pipeline operation is performed at what clock cycle for each instruction of the code snippet. Assume an empty pipeline before starting the execution. State the total number of needed clock cycles for the execution of the code snippet for both approaches.
- (d) Rewrite the source code to solve the problem purely in software.
- (e) What defines the programmer's visible architectural state?

```
ADDI x2, x1, 0 # I1
ADDI x3, x1, 5 # I2
ADDI x4, x3, 3 # I3
ADDI x5, x1, 7 # I4
```



## Q3. (10 points) Assembly:

- (a) Transform the following C-code to RISC-V assembly. All local variables of the C-code **must** be allocated on the stack. The global variable **g** is located at address 0xF00. The RISC-V calling convention must be followed. The assembly startup code including the initialization of the stack is provided below. Write the assembly code for the two functions at the foreseen locations.
- (b) Draw the stack including known values, variable names, stack/frame pointer for the following locations in the program:
  - i. After the last instruction of the prologue of main.
  - ii. Before the call instruction in main and before the first instruction of add.

```
Assembly Reference
  // Located at memory address OxFOO
  int g;
                                                        rd, imm(rs1)
                                                LW
                                                SW
                                                        rs1,imm(rs2)
  int add(int* p) {
    return *p + g;
                                                ADD
                                                        rd,rs1,rs2
                                                ADDI
                                                       rd, rs1, imm
  int main() {
                                                SUB
                                                        rd,rs1,rs2
    int a = 3;
                                                JAL
                                                        rd, imm
    g = 4;
                                                JALR
                                                       rd, imm(rs1)
    return add(&a);
                                                    main:
_start:
 ADDI sp, zero, 0x700
 JAL ra, main
 EBREAK
 add:
```

## Q4. (10 points) **IPv4:**

- (a) How many addresses are assigned to an IPv4 network with subnet mask 255.255.255.224? [1 point] Give the CIDR suffix for this IPv4 network. [1 point]
- (b) What does TTL stand for? [1 point] Which problem does this header field solve? How? [2 points]
- (c) A router implements NAT and wants to forward a packet to a host. Hence, the destination IP address is replaced. What else needs to be done? Which header field(s) are affected? [2 points]
- (d) Explain the SMURF attack [3 points]

 $\rightarrow$ 

## Q5. (10 points) **HTTP & DNS:**

- (a) Explain idempotence in the context of HTTP. Is HTTP OPTIONS idempotent? [2 points]
- (b) List and explain the new features introduced by HTTP 2.0 [4 points]
- (c) What is the purpose of a non-authoritative name server? [1 point]
- (d) Give three examples of ccTLDs [3 points]